Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Currently amended) A method, comprising:

calculating a variation between an input data rate and a pre-determined output data rate, the input data rate being based on a number of data read requests, wherein calculating the variation comprises updating a counter value representative of the variation[[;]], ~~and~~ wherein calculating the variation further comprises:

determining a difference between a total bit group of data received from an input first-in-first-out (FIFO) and a pre-determined output data bus width; and

subtracting the difference from the counter value to update the counter value; and

compensating for the variation by modifying the number of data read requests, and wherein compensating for the variation comprises:

masking a data read request to be transmitted to the input FIFO when the counter value is either equal to or less than a lower threshold value; and

generating an additional data read request to be transmitted to the input FIFO when the counter value is either equal to or greater than an upper threshold value.

2. (Original) The method of claim 1, wherein the variation is compensated to increase a bandwidth in a communication channel.

3. (Original) The method of claim 1, wherein the variation is compensated to increase the bandwidth in a plurality of communication channels.

4. (Original) The method of claim 1, wherein the variation is compensated to decrease a number of idle cell insertions.

5. (Currently amended) The method of claim 1, wherein modifying the number of data read requests comprises generating a plurality of additional data read requests when the counter value is either equal to or greater than an upper threshold value.

6. (Currently amended) The method of claim 1, wherein modifying the number of data read requests comprises masking a plurality of data read requests when the counter value is either equal to or less than a lower threshold value.

7. (Currently amended) The method of claim 1, ~~wherein calculating the variation further comprises:~~

~~determining a difference between a total bit group of data received from an input first in first out (FIFO) and a pre-determined output data bus width; and~~

~~subtracting the difference from the counter value to update the counter value, and wherein compensating for the variation comprises:~~

~~masking a data read request transmitted from a packet encapsulator to the input FIFO when the counter value is either equal to or less than the~~

~~lower threshold value,~~ wherein the lower threshold value is the negative value of the pre-determined output data bus width,[[;]] and

~~generating an additional data read request to be transmitted from the packet encapsulator to the input FIFO when the counter value is either equal to or greater than the upper threshold value,~~ wherein the upper threshold value is the positive value of the pre-determined output data bus width.

8. (Canceled)

9. (Currently amended) The method of claim 1, further comprising:

transmitting an output data stream to an output ~~first-in-first-out (~~FIFO~~)~~;

determining when the output FIFO is substantially full;

passing the data read requests to [[an]] the input FIFO when the output FIFO is not substantially full; and

masking the data read request to the input FIFO when the output FIFO is substantially full.

10. (Previously Presented) The method of claim 9, wherein substantially full is a set value determined using a value representative of an amount of data contained in a number of stages of a pipeline subtracted from another value representative of a capacity of the output FIFO.

11. (Currently amended) The method of claim 1, further comprising:

comparing a total bit group of data received by a packet encapsulator from [[a]] the data read request with a counter value; and

performing at least one of said masking [[a]] the data read request and said generating [[an]] the additional data read request.

12. (Original) The method of claim 11, wherein the total bit group of data is a byte.

13. (Currently amended) The method of claim 11, further comprising passing the data read request to [[an]] the input ~~first-in-first-out (~~FIFO~~)~~.

14. (Currently amended) The method of claim 11, further comprising passing the data read request and the additional data read request to [[an]] the input ~~first-in-first-out (~~FIFO~~)~~.

15. (Currently amended) An apparatus, comprising:

an input first-in-first-out (FIFO) to receive input data at an input data rate;

an encapsulator engine coupled to the input FIFO; and

a packet pre-processor coupled to the encapsulator engine[[,]] and the input FIFO, wherein the packet pre-processor is configured to calculate a variation between [[an]] the input data rate and a pre-determined output data rate and to update a counter value representative of the variation, the input data rate being based on a number of data read requests, wherein the packet pre-processor calculates the variation by determining a difference between a total bit group of data received from the input FIFO and a pre-determined output data bus width, and subtracting the difference from the counter value to update the counter value, wherein the packet pre-processor is configured to compensate for the variation by modifying the number of data read requests, ~~wherein the packet pre-processor is configured to compensate for the variation by~~including,[[:]]

masking a data read request transmitted to the input FIFO when the counter value ~~is either equal to or less than a lower~~ exceeds a first value of a predetermined range ~~threshold value~~[[;]], and

generating an additional data read request transmitted to the input FIFO when the counter value exceeds a second value of the predetermined range. ~~is either equal to or greater than an upper threshold value.~~

16. (Currently amended) The apparatus of claim 15, wherein the packet pre-processor comprises:

a pre-compute circuitry coupled to the input FIFO and the encapsulator engine, wherein the pre-compute circuitry is configured to calculate [[a]] the total bit group of data received by the packet pre-processor at the input data rate; and

a request modifier circuitry coupled to the pre-compute circuitry and the input FIFO, wherein the request modifier circuitry is configured to determine [[a]] the difference between the -total bit group of data calculated by the pre-compute circuitry and [[a]] the pre-determined output data bus width.

17. (Currently amended) The apparatus of claim 16, further comprising:

a link layer device coupled to the input FIFO; and

~~an input first in first out (FIFO) coupled to the request modifier circuitry, link layer device and the pre-compute circuitry, the input FIFO to receive input data at the input data rate; and~~

an output FIFO coupled to the encapsulator engine and the request modifier circuitry, wherein the output FIFO is configured to transmit output data at the pre-determined output data rate.

18. (Original) The apparatus of claim 17, further comprising:

a framer engine coupled to the output FIFO; and

a physical interface device coupled to the framer engine.

19. (Original) The apparatus of claim 18, wherein the pre-compute circuitry receives input data from the input FIFO, the encapsulator engine receives the input data from the pre-compute circuitry, the output FIFO receives the output data from the encapsulator engine, the request modifier circuitry receives data read requests from the framer engine, the link layer device receives the data read requests from the request modifier circuitry.

20. (Currently amended) An apparatus, comprising:

means for transmitting data through a communication channel having a bandwidth;

an input first-in-first-out (FIFO) to receive input data from the communication channel at an input data rate;

means for determining a difference between a total bit group of data received from the input FIFO and a pre-determined output data bus width to ~~calculating~~ calculate a variation between [[an]] the input data rate and a pre-determined output data rate, the input data rate being based on a number of data read requests; ~~and~~

means for subtracting the difference from a counter value representative of the variation;

means for masking a data read request transmitted to the input FIFO when the variation exceeds a first threshold value of a pre-determined range to ~~means for compensating~~ compensate for the variation to increase a utilization efficiency of the bandwidth~~, wherein the means for compensating for the variation comprises:~~; and

means for generating an additional data read request transmitted to the input FIFO when the variation exceeds a second threshold value of the pre-determined range to compensate for the variation to increase the utilization efficiency of the bandwidth.

21. (Currently amended) The apparatus of claim 20, wherein the means for ~~compensating~~ masking and the means for generating decreases a number of idle cell insertions.

22. (Currently amended) The apparatus of claim 20, wherein the means for ~~compensating~~ masking and the means for generating compensates for invalid bytes of an input data stream.

23. (Currently amended) A system, comprising:

a link layer device;

a first physical interface device; and

a framer coupled to the link layer device and the first physical interface device, wherein the framer comprises an input first-in-first-out (FIFO), an encapsulator engine, and a packet pre-processor coupled to the encapsulator engine and the input FIFO, wherein the packet pre-processor is configured to calculate a variation between an input data rate and a pre-determined output data rate and to update a counter value representative of the variation, the input data rate being based on a number of data read requests, wherein the packet pre-processor calculates the variation by determining a difference between a total bit group of data received from the input FIFO and a pre-determined output data bus width, and subtracting the difference from the counter value to update the counter value, wherein the packet pre-processor is configured to compensate for the

variation by modifying the number of data read requests, ~~wherein the packet pre-processor is configured to compensate for the variation by:~~ including,

masking a data read request transmitted to the input FIFO when the counter value ~~is either equal to or less than a lower threshold value~~ exceeds a first value of a predetermined range; and

generating an additional data read request transmitted to the input FIFO when the counter value ~~is either equal to or greater than an upper threshold value~~ exceeds a second value of the predetermined range.

24. (Currently amended) The system of claim 23, wherein the packet pre-processor comprises:

a pre-compute circuitry coupled to the input FIFO and the encapsulator engine, wherein the pre-compute circuitry is configured to calculate [[a]] the total bit group of data received by the packet pre-processor at the input data rate; and

a request modifier circuitry coupled to the pre-compute circuitry and the input FIFO, wherein the request modifier circuitry is configured to determine [[a]] the difference between the total bit group of data calculated by the pre-compute circuitry and [[a]] the pre-determined output data bus width.

25. (Original) The system of claim 24, further comprising a second physical interface device coupled to the link layer device, wherein the second physical interface device, the link layer device, the framer and the first physical interface device reside in a line card.

26. (Original) The system of claim 25, wherein the second physical interface device is an Ethernet device and the first physical interface device is a Synchronous Optical Network (SONET) device.

27. (Original) The system of claim 25, wherein the line card is coupled to a wide area network (WAN).

28. (Currently amended) A method, comprising:

calculating a variation between an input data rate and a pre-determined output data rate, the input data rate being based on a number of data read requests, wherein calculating the variation comprises updating a counter value representative of the variation[[;]], ~~and~~ wherein calculating the variation further comprises:

determining a difference between a total bit group of data received from an input first-in-first-out (FIFO) and a pre-determined output data bus width; and

subtracting the difference from the counter value to update the counter value; and

compensating for the variation by modifying the number of data read requests, and wherein compensating for the variation comprises:

masking a data read request to be transmitted to the input FIFO when the counter value is either equal to or greater than an upper threshold value; and

generating an additional data read request to be transmitted to the input FIFO when the counter value is either equal to or less than a lower threshold value.

29. (Currently amended) The method of claim 28, ~~wherein calculating the variation further comprises:~~

~~determining a difference between a total bit group of data received from an input first-in-first-out (FIFO) and a pre-determined output data bus width; and~~

~~subtracting the difference from the counter value to update the counter value, and wherein compensating for the variation comprises:~~

~~masking a data read request transmitted from a packet encapsulator to the input FIFO when the counter value is either equal to or greater than the upper threshold value,~~ wherein the upper threshold value is the positive value of the pre-determined output data bus width,[[;]] and

~~generating an additional data read request to be transmitted from the packet encapsulator to the input FIFO when the counter value is either equal to or less than the lower threshold value,~~ wherein the lower threshold value is the negative value of [[a]] the pre-determined output data bus width.